**CMPEN 371: Advanced Digital Design**

**Fall 2016**

**Lab 4: Sequential Components**

**Due: 28 September 2016**

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**ACKNOWLEDGEMENT**

This work is entirely our own and I did not provide any assistance except as noted. The approximate contribution of each team member is as follows:

100% Saw Xue Zheng \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Grading Rubric**

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| --- | --- |
| **Criteria** | **Grade** |
| Design (Sound algorithm, good block diagrams / state diagrams / state tables, efficient design, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Translate to VHDL (VHDL matches design docs, good comments / whitespace, follows guidelines, efficient coding, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Test in Simulator (test bench or script for each component and FSM, good coverage, components / FSMs verified, etc.)  Excellent: 3; Good: 2; Satisfactory: 1; Unsatisfactory: 0; Failure: -1 or worse | / 3 |
| Test in Hardware (demo in lab)   * Registers work as specified * 8-digit 7-segment displays cleanly (no flicker or ghosting) shows proper values * LEDs show the value of register 0 * Other | / 35 |
| Bonus (optional challenge, etc.) |  |
| Penalty (late demo, late submission on ANGEL, team member absent from demo, etc.)  Demo late in lab: -2; Demo up to 5 days late: -5; Demo more than 5 days late: -10  Submitted late or incompletely on ANGEL: -5; Not submitted on ANGEL: no grade for lab |  |
| TOTAL | / 50 |

**DESIGN**

The following design documents are attached:

Filename Description

L04\_D01.pdf Top level block diagram.

L04\_D02.pdf Block diagram for Counter and Pulse Generator.

L04\_D03.pdf Block diagram for WordTo8dig7seg.

**TRANSLATE TO VHDL**

The following HDL models are attached:

Filename Description

Lab04\_xps5001.vhd Top Level: Top Level for Lab04

PulseGenerator.vhd Component: Pulses every maxCount+1 count.

Debounce.vhd Component: Debounce the input signal.

OneShot.vhd Component: OneShot the input signal

WordTo8dig7seg.vhd Component: Convert 32-bit word to 8 digit 7 seven segment display driver

The following HDL models and other files are not attached but are submitted electronically:

Filename Description

Counter.vhd n-bit counter counts up to 2^n numbers.

Reg.vhd n-bit register.

Reg\_SIPO.vhd n-bit shift register serial in parallel out.

**TEST IN SIMULATOR**

*None. The test was conducted by programming the board and testing it manually. An eightdigitseven7\_test.bit is attached which demonstrates the eight digit seven segment display working. The corresponding .vhd file is attached.*

**TEST IN HARDWARE**

*The project implements all the functionality specified in the lab handout.*

**PERFORMANCE**

The following cost and performance metrics were obtained:

Area (resources used)

Number of Slice Registers: 202

Number of Slice LUTs: 262

Delay

Minimum Period: 5.537 ns

Maximum Frequency 180.6 MHz

The critical path goes from *pulse\_gen\_200hz/count/Q\_int\_17*, through *CompareEQU and Debouncer* to *dbounced/Dflop2/Q*

**QUESTIONS**

A two bit counter can be used effectively to divide the 100MHz clock to generate a pulse every 50MHz.